CLAIMS

1. A data processor comprising, at least, a CPU for controlling an entire system, a DSP for performing preset processing, and an external memory to be accessed by the DSP and to be capable of being accessed through the DSP by the CPU;

the DSP being configured to have at lease two bus cycles as a unit of one data access, the number of the bus cycles used in the unit of one data access being selectable, and a data length to be accessed to the external memory being variable;

the DSP including:

a determination means for determining whether the DSP is accessing to the external memory or not;

a control means for determining whether the CPU is allowed to access the external memory, based on the presence and absence of a signal from a determination means; and

means for performing a switching operation of an address and a data in connection with the external memory according to a command from the control means, and inputting or outputting the address and the data based on the switching operation;

wherein in a case where the data length is selected so as to perform accessing by a maximum number of the bus cycles, when the determination means determines that the DSP is accessing the external memory, access from the CPU

to the external memory is placed in a wait state by the control means, and in a case where the data length is not selected so as to perform accessing by a maximum number of the bus cycles, the control means allows the CPU to access the external memory by utilizing a free bus cycle.

2. A data processor comprising, at least, a CPU for controlling an entire system, a sound source for supplying a musical tone signal, a DSP for performing preset processing to apply a desired effect to the musical tone signal supplied from the sound source, and an external memory to be accessed by the DSP and to be capable of being accessed through the DSP by the CPU;

the DSP being configured to have at lease two bus cycles as a unit of one data access with respect to signal processing of the musical tone signal, the number of the bus cycles used in the unit of one data access selectable, and a data length to be accessed to the external memory being variable;

the DSP including:

a determination means for determining whether the DSP is accessing to the external memory or not;

a control means for determining whether the CPU is allowed to access the external memory, based on the presence and absence of a signal from a determination means; and

means for performing a switching operation of an address and a data in connection with the external memory

according to a command from the control means, and inputting or outputting the address and the data based on the switching operation;

wherein in a case where the data length is selected so as to perform accessing by a maximum number of the bus cycles, when the determination means determines that the DSP is accessing the external memory, access from the CPU to the external memory is placed in a wait state by the control means, and in a case where the data length is not selected so as to perform accessing by a maximum number of the bus cycles, the control means allows the CPU to access the external memory by utilizing a free bus cycle.

3. A data processor having a fixed number of memory access timings per sampling cycle and comprising a plurality of DSPs for accessing a single external memory in a single package;

the data processor further comprising:

a read/write control means, which when each of the DSPs issues a read command or a write command at the same timing, controls the command of which DSP is allowed;

an access determination means, which when each of the DSPs issues a read command or a write command in the timing, determines which DSP is allowed to perform memory access;

a first selector for outputting an address from the allowed DSP in response to a determination signal from the access determination means; and

a second selector for outputting a data from the allowed DSP in response to the determination signal; and

each of the DSPs including a control means for data acquisition, which acquires a data from the external memory in response to the determination signal from the access determination means.

4. The data processor according to Claim 3, wherein the read/write control means does not access the external memory when the respective DSPs issue plural commands.

5. A data processor having a fixed number of memory access timings per sampling cycle and comprising a plurality of DSPs for accessing a single external memory in a single package, the external memory storing musical tone waveform data;

the data processor further comprising:

a read/write control means, which when each of the DSPs issues a read command or a write command at the same timing, controls the command of which DSP is allowed;

an access determination means, which when each of the DSPs issues a read command or a write command in the timing, determines which DSP is allowed to perform memory access;

a first selector for outputting an address from the allowed DSP in response to a determination signal from the access determination means; and

a second selector for outputting a data from the allowed DSP in response to the determination signal; and

each of the DSPs including a control means for data acquisition, which acquires a data from the external memory in response to the determination signal from the access determination means.

6. The data processor according to Claim 5, wherein the read/write control means dose not access the external memory when the respective DSPs issue plural commands.